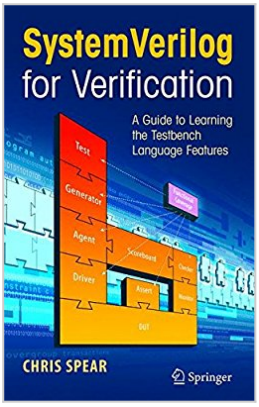

SystemVerilog for Verification: A Guide to Learning the Testbench Language Features

By Chris Spear

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SystemVerilog for Verification teaches the reader how to use the power of the new SystemVerilog testbench constructs plus methodology without requiring in-depth knowledge of Object Oriented Programming or Constrained Random Testing. The book covers the SystemVerilog verification constructs such as classes, program blocks, C interface, randomization, and functional coverage. **SystemVerilog for Verification** also reviews some design topics such as interfaces and array types. There are extensive code examples and detailed explanations. The book will be based on Synopsys courses, seminars, and tutorials that the author developed for SystemVerilog, Vera, RVM, and OOP. Concepts will be built up chapter-by-chapter, and detailed testbench using these topics will be presented in the final chapter. **SystemVerilog for Verification** concentrates on the best practices for verifying your design using the power of the language.

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